DATA SHEET

Micro Devices

MD1212 FUZZY DATA CORRELATOR

FEATURES

- Low Power CMOS Technology
- Both Match Flag and Correlation Scores are Available
- Adjustable Match Threshold
- 128-Bit Data Comparisons
- Bits May Be Selectively Masked
- Easily Expanded to any Word Length by Cascading Devices
- Standard 8-Bit Microprocessor Bus Interface
- Standard 28-Pin DIP

APPLICATIONS

- Image Comparison and Recognition
- Radar/Sonar Pattern Matching
- Error Correction Coding
- Data Synchronization
- Flag Word Detection
- Check Sorting Equipment
- Bar Code Identification
- Video Frame Synchronization
- Time Delay Measurement

The **MD1212** is a high-speed programmable CMOS Fuzzy Data Correlator based on a parallel structure 128-input Hamming comparator. The MD1212 is intended for real time data and image processing systems. The device is so named as its adjustable correlation threshold allows the degree of acceptable correlation to be selected by the user.

The Fuzzy Data Correlator uses an internal pipeline to achieve rapid correlation results. With the device placed in the exact match mode and using a 50MHz clock, the match flag is valid in 35ns after data input. For threshold values greater than zero, the match flag and correlation score are valid in 55ns.

The MD1212 is easily expanded to handle any word length without sacrificing speed, by simply cascading devices.

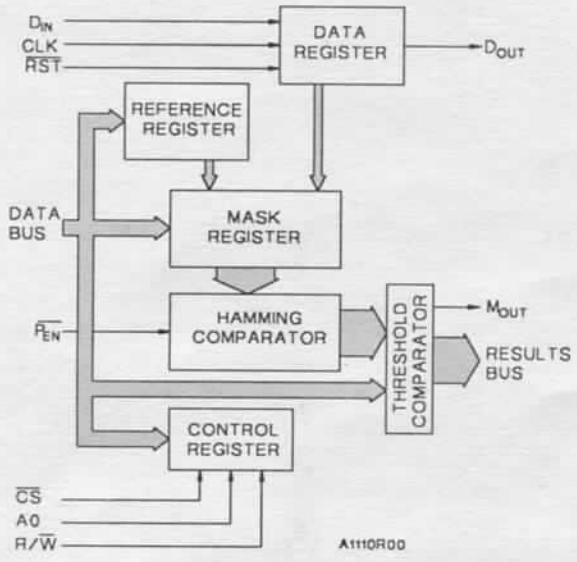


Figure 1. MD1212 Block Diagram

Connection Diagram
28 Pin DIP

CHARACTERISTICS

Absolute Maximum Ratings (T_A=25°C)

Power Supply Voltage, V_{CC}	-.5 to 7VDC
Power Supply Current, I_{CC} (1)	300mA
Operating Temperature, T_{OPT}	0 to 70°C
Storage Temperature, T_{STG}	-65 to 150°C
Clock Speed	50MHz

Note: (1) I_{CC} = 4.5nA/Hz

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.75	5.25	VDC
All Inputs and Outputs		-.5	5.5	V
Output Load Capacitance			50	pF
Ambient Temperature	T_A	0	70	°C

DC Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Low-level Output Voltage (1)(2)(3)	V_{OL}			.3 V_{DD}	V	V_{CC}=5V I_{OL}=0mA
High-level Output Voltage (1)(2)	V_{OH}	.7 V_{DD}			V	V_{CC}=5V I_{OH}=0mA
Low-level Output Current (1)	I_{OL}	12			mA	V_{OL}=.4V
High-level Output Current (1)	I_{OH}	6.4			mA	V_{OH}=2.4 V
Low-level Output Current (2)(3)	I_{OL}	6			mA	
High-level Output Current (2)	I_{OH}	3.2			mA	
Low-level Input Voltage (4)(5)	V_{IL}	0		.8	V	V_{CC}=5V
High-level Input Voltage (4)(5)	V_{IH}	2.2		5	V	V_{CC}=5V
Tri-state Leakage Current (1)	I_{LO}		10		µA	V_{OUT}= 0 to 5V
Low-level Input Voltage (1)	V_{IL}			.3 V_{DD}	V	V_{CC}=5V
High-level Input Voltage (1)	V_{IH}	.7 V_{DD}			V	V_{CC}=5V

Notes:
(1) Applies to DB(0-7)
(2) Applies to RS(0-7) and D
(3) Applies to M_{OUT}
(4) Applies to CLK and D_{IN}
(5) Applies to A0, $\overline{CS}$, $\overline{RST}$, $\overline{P_{EN}}$ and R/$\overline{W}$

Pin Descriptions

D_{IN} Serial Data Input. Data input to the 128-bit shift register.

D_{OUT} Output of the 128-bit shift register.

CLK Data Clock. Clocks data through the shift register, pipeline registers, results bus and match output.

$\overline{CS}$ Chip Select input used to enable the device for external processor access.

A0 Register select pin (used in conjunction with R/$\overline{W}$):
A0=0: Write control register, read results register.
A0=1: Write data to selected register (Reference, Mask, or Threshold register). Read M_{OUT} bit.

DB(7:0) Processor data bus used for writing the control register, data registers, and reading correlation scores and match flag.

R/$\overline{W}$ Read/Write control pin for reading and writing the registers in the FDC.
R/$\overline{W}$=1 Read Mode
R/$\overline{W}$=0 Write Mode (data latched on rising edge of R/$\overline{W}$)

$\overline{RST}$ Data register reset. Used to reset the contents of the data shift register. RST must be held low for four clock cycles in order to fully reset the data shift registers.

$\overline{P_{EN}}$ Pipe enable (active low), enables pipelining in the FDC to allow for data correlation at speeds up to 50MHz.

M_{OUT} Match output flag. Match is controlled by the threshold register. If the correlation score is ≤ the threshold value, the match output pin remains high. When the score exceeds the threshold the output pulls low. This output is open collector and requires an external pull-up to V_{CC}.
M_{OUT}=0 No match
M_{OUT}=1 Match

RS(7:0) Results Bus. 8-bit binary correlation score output updated by clock.

DESCRIPTION

MD1212 Signals

Signal Name	Pin #	Signal	Direction
DB0	3	Processor	Input/Output
DB1	4	Data Bus	
DB2	5		
DB3	6		
DB4	8		
DB5	9		
DB6	10		
DB7	11		
RS0	26	Results	Output
RS1	25	Bus	
RS2	24		
RS3	23		
RS4	22		
RS5	21		
RS6	20		
RS7	19		
D_{OUT}	27	Data Out	Output
M_{OUT}	18	Match	Output
CLK	1	System Clock	Input
$\overline{RST}$	15	Reset	Input
$\overline{P_{EN}}$	16	Pipe Enable	Input
$\overline{CS}$	13	Chip Select	Input
A0	12	Address 0	Input
R/$\overline{W}$	17	Read/Write	Input
D_{IN}	2	Serial Data	Input
VCC	28	+5 Volts	
GND	14		
GND	7		

General

The MD1212 Fuzzy Data Correlator (FDC) is a 128-bit data correlator designed for use in applications where high speed (up to 50MHz) data streams must be correlated. To achieve the high speed performance of the MD1212, the Hamming distance between input and reference data pattern is computed using a massively parallel comparison architecture. This design approach is based on neural network techniques, and delivers superior performance while reducing internal complexity and allowing the use of mature IC processes.

Device operation is controlled through a standard microprocessor compatible interface. Reference and mask registers, threshold registers, and operational modes are accessible through the processor interface. The MD1212 supports cross-correlation and autocorrelation operations at speeds up to 50MHz.

The FDC is controlled by means of an internal control register and external pins. The operating modes fall into two classes; processor interface and correlation modes. FDC control modes are stored in an internal eight bit control register which is written by the processor (Figure 2). Correlation functions are controlled with a combination of the control registers MSB (bit 7) and the pipe enable ($\overline{P_{EN}}$) pin.

MSB **Control Register** LSB

7	6	5	4	3	2	1	0
EMC	AINC	RS1	RS0	RA3	RA2	RA1	RA0

RA_0-RA_3: Internal Data Register Address (1 of 16).

RS_0-RS_1: Register Select

RS1	RS0	Register
0	0	None
0	1	Mask Register
1	0	Reference Register
1	1	Threshold Register

AINC: Auto Address Increment

EMC: Exact Match Mode

Figure 2. Control Register

Functional Description

Data enters the MD1212 though the serial input D_{IN}, on the rising edge of clock (CLK). The data is shifted into a 128-bit serial in parallel out (SIPO) register (Figure 3). The last stage of the SIPO is tied to the D_{OUT} pin for expansion of the correlator beyond 128-bits (Figure 11). As data is shifted into the device it is compared with the contents of the 128-bit Reference register. At each clock time the serial data and the

DESCRIPTION

reference data are compared by an XOR array. Differences between the reference bits and the data bits generate an error value. The output of each XOR comparator is ANDed with a corresponding bit from the Mask register. The Mask register is used to mask "don't cares" (bits which the user does not care about in the comparison). Writing a Mask bit to a 0(low) masks that bit from the comparison. In this way, the user may select only those input bits which are pertinent to the correlation.

After masking, the error bits are summed to give the resulting correlation score which represents the number of mis-matches between the data and reference patterns. In applications where the correlation score must represent the number of matches, the input data stream need only to be inverted.

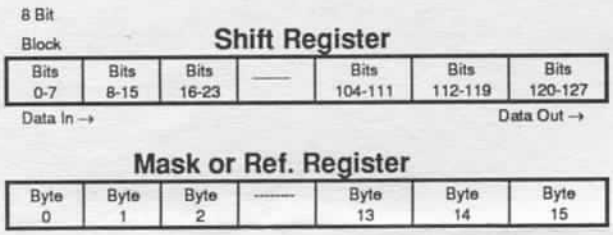


Figure 3. Reference/Mask Register

Processor Interface

The Reference, Mask, Control and Threshold registers are written in the MD1212 via a standard 8-bit microprocessor interface. Handshaking is controlled with the Chip Select pin ($\overline{CS}$) which enables the device for processor access. Along with the R/$\overline{W}$ bit, address (A_0) selects writing to the control register (A_0=0) or the data registers (A_0=1) and reading the results register (A_0=0) or reading the status of the match interrupt (A_0=1). The rising edge of Read/Write signal (R/$\overline{W}$) latches the data from the data bus (DB(7:0)) into the internal registers at the end of the processor write time (R/$\overline{W}$=0).

The Mask and Reference registers in the MD1212 are addressable in 8-bit bytes (16 addresses total). The Threshold register is a single 8-bit register. The Control register governs the following; register address selection, register selection, auto increment mode control, and exact match mode operation. An outline of the control register is shown in Figure 2. The processor selects which register to write to by first writing the control register with the register select and register address. Bits 0-3 (RA_0-RA_3) set the register address and bits 4 and 5 (RS_0 & RS_1) select which register to write. Bit 6 (AINC) enables the auto address increment feature.

Upon selecting the Auto increment mode, register address bits RA_0-RA_3 are automatically reset to zero. With A_0 and AINC high (logic 1) data may be written to a selected 8-bit register. After the data is written the internal address counter automatically increments to the next consecutive address. In this mode the processor can completely write the Reference or Mask register in 16 write cycles. With the AINC bit low, the register's address must be selected through the control register before the data can be written to that register, requiring two processor cycles to write data to one 8-bit register: one to set up the address, and one to write the data. This mode, though slower than the auto increment mode, allows selective updating of 8-bit portions of the 128-bit registers. Figure 3 diagrams the location of each of the 16 bytes for the reference and mask register with respect to the shift register. In the Auto increment mode, after the byte 15 is written, the address counter rolls over to address 0, thereby allowing the processor to continuously write data to a register. A typical application for this mode of operation is the processor controlled autocorrelation operation.

Bit 7 (EMC) of the control register enables the Exact match mode of operation. In this mode the threshold function is bypassed. The correlation scoring and the threshold comparison function are disabled in this mode.

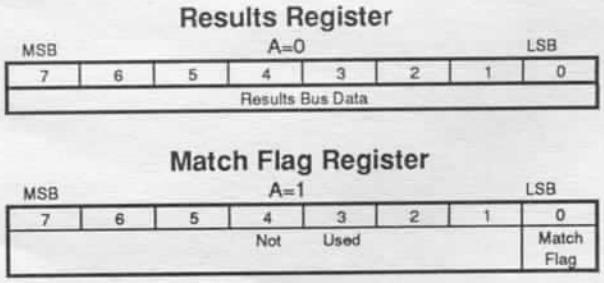


Figure 4.
Results Register and Match Flag

Both the Results register and the Match flag may be read by the processor (Figure 4). The results register contains the value of the results bus associated with

DESCRIPTION

the most recent match condition. The Match flag is the current status of the M_{OUT} pin. They are accessed as described under Processor Interface.

The threshold register (Figure 5) allows the user to control the operation of the M_{OUT} pin. The threshold value is the value which the RS(7:0) bus must be less than or equal to, to be considered a match, resulting in the M_{OUT} pin signalling a match condition. The threshold value is calculated by adding the table value of bits 5, 6 and 7 to the binary value of bits 0 thru 3. If bit 4, the disable bit, is set then no thresholding will occur.

MSB LSB

7	6	5	4	3	2	1	0
A	B	C	Disable	8	4	2	1
Adder			X	Threshold Value			

A	B	C	Add To
0	0	0	0
1	0	0	16
0	1	0	32
1	1	0	48
0	0	1	64
1	0	1	80
0	1	1	96
1	1	1	112

Examples

Register	Value
XXX1XXXX	Disabled
00000110	6
10000110	22
00101001	73

Figure 5. Threshold Register

Correlation Modes

There are two correlation modes; pipelined ($\overline{P_{EN}}$ low) and non-pipelined ($\overline{P_{EN}}$ high). In the pipelined mode correlation results and the Match flag become valid in the third clock cycle after the data sequence is input (typically 55ns at 50MHz). Once valid, M_{OUT} and the Results bus (RS(7:0)) may be latched using the next rising edge of the clock. Thus the value on the M_{OUT} and the Results bus represent correlation of a data sequence entered three clocks earlier. (See Figure 6)

In the non-pipelined mode the correlation results and the match interrupt are available after the second rising edge of the clock (CLK).

To assure proper operation, the device must be operated in pipelined mode when the input clock exceeds 20MHz.

Reset Function

The data shift register in the FDC can be reset to 0 by bringing the Reset pin ($\overline{RST}$) low and clocking the device a minimum of four times. This allows the user to initialize the device quickly.

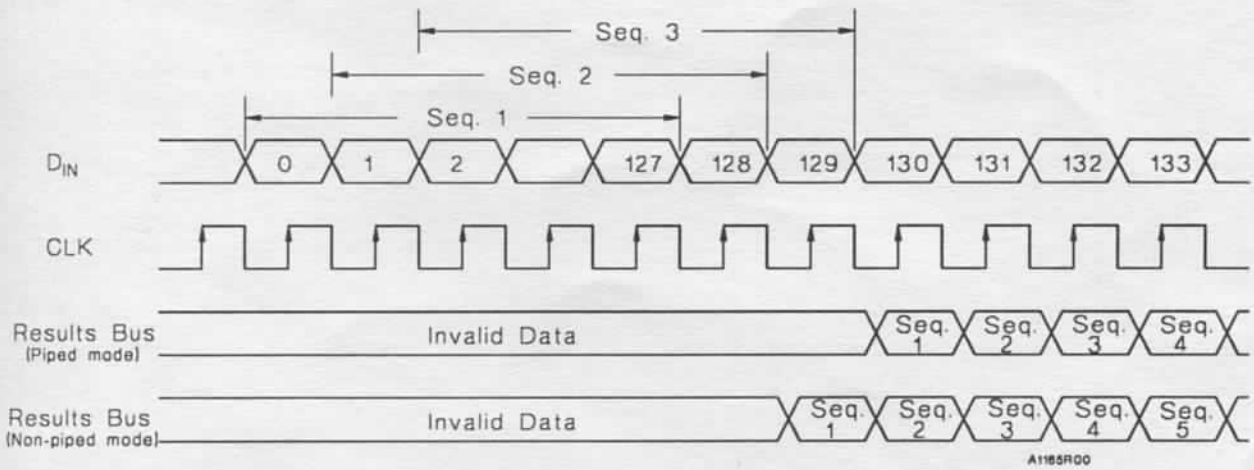
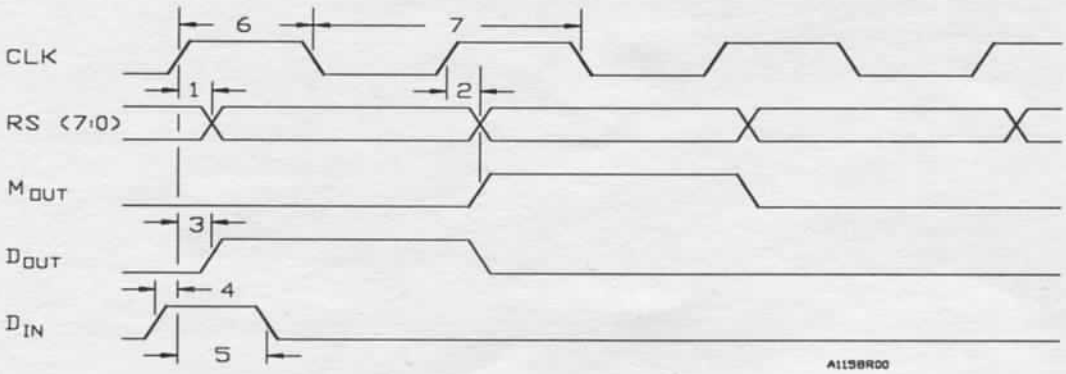


Figure 6. Results Bus Data Sequence

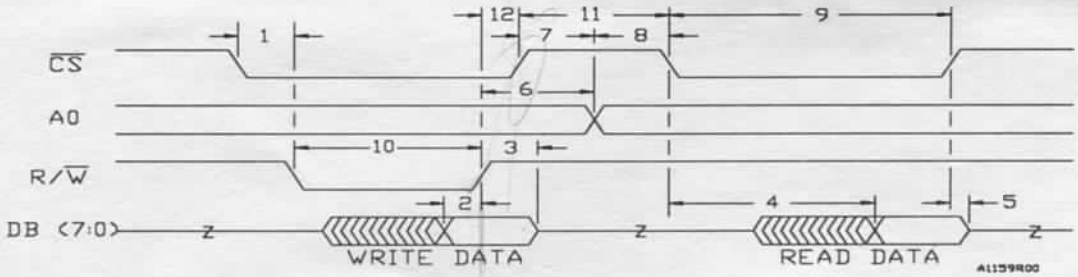
TIMING DIAGRAMS



AC Characteristics T_A=0 to +70°C V_{CC}=5VDC±10% C_L=25pF

No.	Signal	Description	Min	Typ	Max	Notes
1	$T_{pd}CLK(RS)$	CLK to Results Delay		15ns	22ns	Typical Spec. @ T_A=+25°C
2	$T_{pd}CLK(M_{out})$	CLK to M_{out} Delay		15ns	20ns	500Ω Pullup
3	$T_{pd}CLK(D_{out})$	CLK to D_{out} Delay		10ns	15ns	
4	$T_{sw}CLK(D_{IN})$	CLK to D_{IN} Setup Time	5ns			
5	$T_HCLK(D_{IN})$	CLK to D_{IN} Hold Time	5ns			
6	T_{pw}	Pulse Width		10ns		Applies to All Inputs
7	T_pCLK	Clock Period		20ns		

Figure 7. Data Input Timing



AC Characteristics T_A=0 to +70°C V_{DD}=5VDC C_L=25pF

No.	Signal	Description	Min	Max	Notes
1	$T_d\overline{CS}(R\overline{W})$	$\overline{CS}$ to R/$\overline{W}$ Delay	5ns		
2	$T_{su}DB(R\overline{W})$	Data Setup Time	5ns		
3	$T_HDB(R\overline{W})$	Data Hold Time	10ns		
4	$T_d\overline{CS}(DBr)$	$\overline{CS}$ to Data Read Delay		20ns	
5	$T_d\overline{CS}(DBt)$	$\overline{CS}$ to Data Tri-state		10ns	
6	$T_dR\overline{W}(A0)$	R/$\overline{W}$ to A0 Delay	10ns		
7	$T_d\overline{CS}(A0)$	$\overline{CS}$ to A0 Delay	10ns		
8	$T_dA(CS)$	A0 to CS Delay	10ns		
9	$T_W\overline{CS}$	Pulse Width $\overline{CS}$	25ns		
10	$T_WR\overline{W}$	Pulse Width R/$\overline{W}$	20ns		
11	$T_c\overline{CS}$	$\overline{CS}$ Cycle Time	20ns		
12	$T_HR\overline{W}(cs)$	R/$\overline{W}$ to $\overline{CS}$ Hold Time	5ns		

Minimum pulse width on any pin is 10ns unless otherwise noted.

Figure 8. Processor Interface Timing

APPLICATIONS

The MD1212 is intended for use in systems which require preprocessing of data. The MD1212 could be used to synchronize or flag a pattern recognition system. The MD1212 architecture is flexible enough to allow it to be used in other systems. Some typical applications follow:

Multi-Bit x 1 Bit Correlation (Figure 9)

Figure 9 illustrates byte-wise correlation, where the MSB correlation scores must be weighed more heavily than the LSB scores. Reference patterns may be written into the FDC's by the µprocessor. Since data is binary, the $\div 2^n$ functions may be accomplished with shifts.

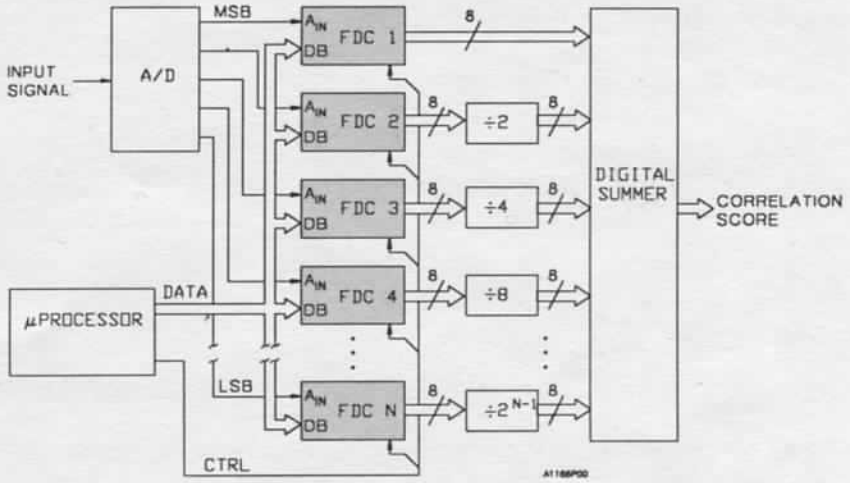


Figure 9. Multi-Bit x 1 Bit Correlation

Detect Header, Grab Data Application (Figure 10)

When a match is found by the FDC it triggers external circuitry to begin storing the data pattern being clocked through the shift register.

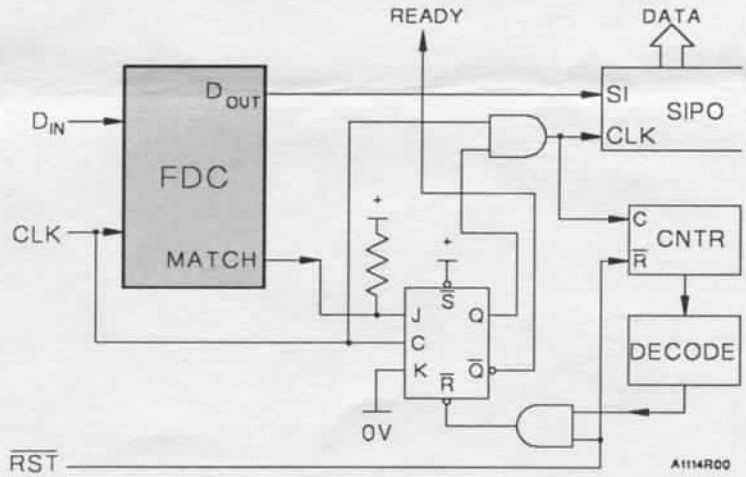


Figure 10. Detect Header, Grab Data Application

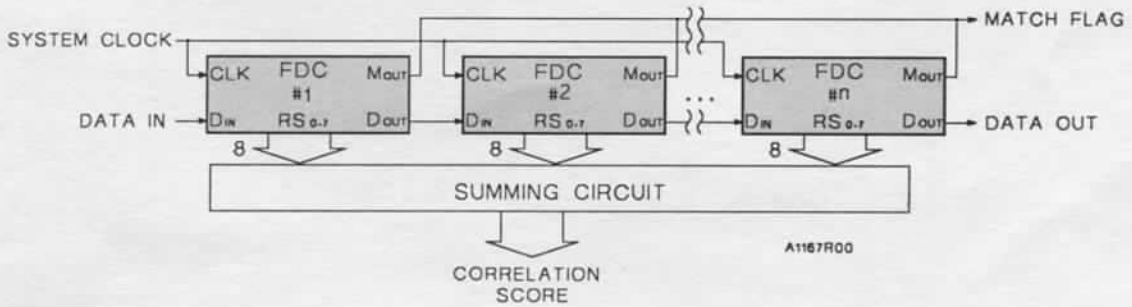


Figure 11. Data Length Expansion Application

Watchdog/Sync Pulse Generation (Figure 12)

Having loaded the reference register with the pattern to be searched for, each time the pattern is detected the M_{OUT} pin will pulse high providing a watchdog/synchronizing pulse.

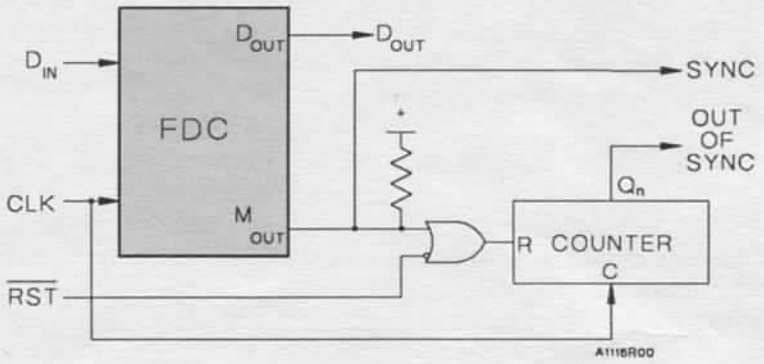
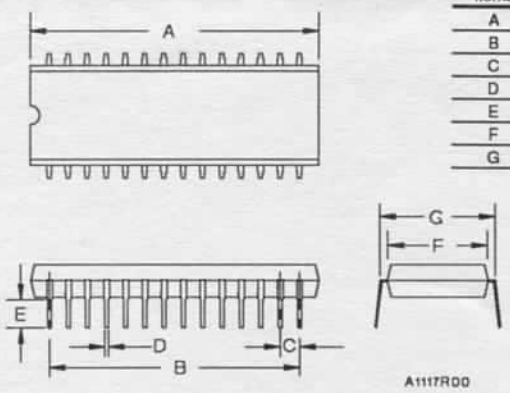


Figure 12.
Watchdog/Sync Pulse Generation Application

Other applications include: Ranging and Time Measurement Systems, and Communication Receivers.



Items	Millimeters	Inches
A	38.1 max	1.5 max
B	33.02	1.3
C	2.54 typ	.10 typ
D	.5±.10	.02±.05
E	3.6±.3	.142±.012
F	13.2	.52
G	15.24 typ	.60 typ

Package Dimensions
28 Pin DIP

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