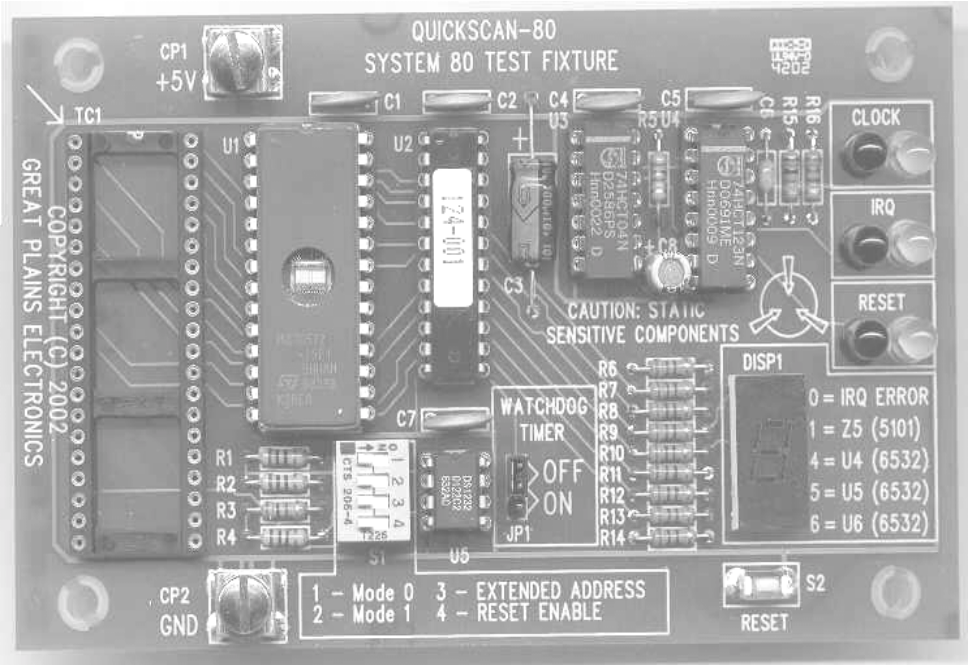
QuickScan80

System 80 Test Fixture



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Introduction

The *QuickScan80* has been developed to quickly identify faults within the major components of the Gottlieb System 80 MPU assembly. The major components tested by the *QuickScan80* are the three RAM, I/O, Timer IC's (RIOT's) and the low power 5101 memory. In the process of testing these components – most other logic devices, including the CPU and decode logic, are also tested. A 7-Segment LED display is used to provide the user with continuous status regarding testing of the MPU assembly. Three pair of red and green LED's are also used to provide the user with instant status of the MPU's Reset, IRQ, and CPU Clock signals.

Important!

Before attempting any testing – verify power supply to be providing +5 volts +/-5%

Never change QuickScan80 settings while power is turned on.

Never change jumpers or connectors while power is turned on.

Both MPU and QuickScan80 contain static sensitive components.
An antistatic wrist strap must be worn when working with these components.

Quick Start

The *QuickScan80* must be properly configured and installed prior to use. Configuration includes proper setting of the DIP Switches and Jumper. Installation includes proper connection of the ribbon cable and jumper wire.

DIP Switch settings:
Standard DIP Switch Settings for using QuickScan80 to test a system 80 or 80A MPU:

DIP Switch Position 1	OFF (open)
DIP Switch Position 2	OFF (open)
DIP Switch Position 3	OFF (open)
DIP Switch Position 4	ON (closed)

Standard DIP Switch Settings for using QuickScan80 to test a system 80B MPU or a System 80 or 80A without vacuum fluorescent displays:

DIP Switch Position 1	ON (closed)
DIP Switch Position 2	OFF (open)
DIP Switch Position 3	OFF (open)
DIP Switch Position 4	ON (closed)

Jumper setting:
An onboard jumper is used to control a 'watchdog' timer on the QuickScan80. For testing purposes, this 'watchdog' timer must be disabled. Move 'Watchdog' jumper to the ***OFF*** position.

Ribbon Cable Installation:

A short 40-position ribbon cable assembly is used to attach the *QuickScan80* to the Gottlieb MPU assembly. To attach the ribbon cable assembly – install ribbon cable such that pin 1 of the connector on the ribbon cable assembly is inserted into pin 1 of the 40-Pin IC sockets (TC1) on both the MPU assembly and the test fixture. Refer to Figure 1 for proper installation of the Ribbon Cable Assembly onto the MPU. Pin 1 on the *QuickScan80* is easily identified with the silk-screened arrow. ***Warning – Incorrect installation of the ribbon cable assembly can result in damage to the MPU assembly and/or the QuickScan80. Verify proper installation of ribbon cable before applying power. Only install or remove the ribbon cable assembly when power has been turned off. When removing the ribbon cable assembly - never pull by the ribbon cable!*** Insert a flat bladed screwdriver under the ribbon cable connector and gently pry loose. To prolong the life of the ribbon cable, it is recommended that the ribbon cable only to be removed from the MPU and not removed from the *QuickScan80.*

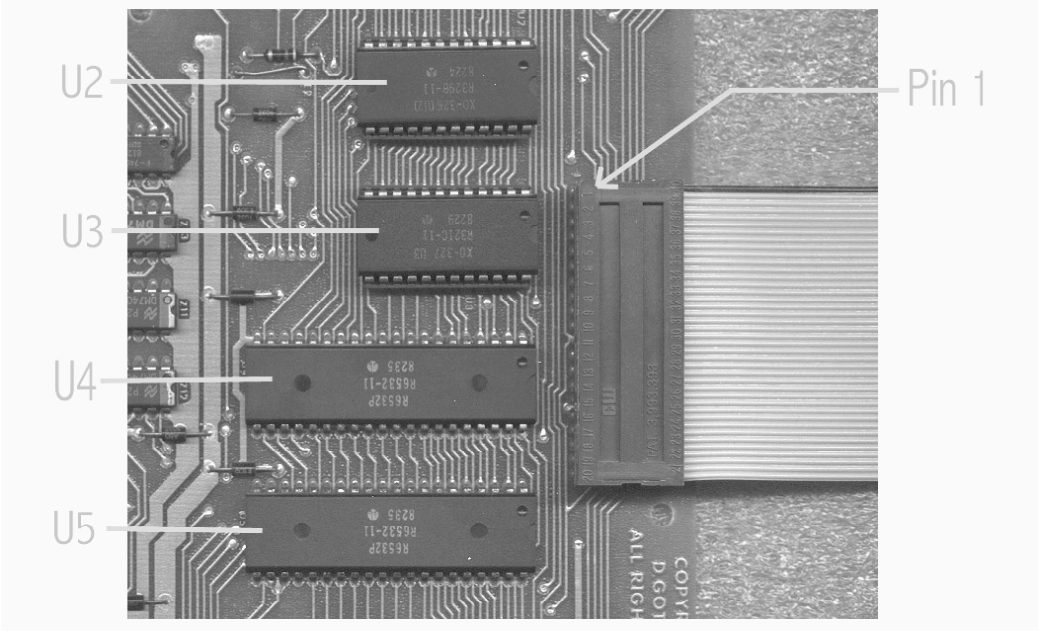


Figure 1 – Installation of Ribbon cable onto TC1 of MPU assembly

Jumper Wire Installation:

For System 80 and 80A machines:

In order for the *QuickScan80* test fixture to properly insert code into the MPU assembly - the existing U2 and U3 ROM's must be disabled. To perform this disabling, the ROM select signal on the MPU must be grounded. Attach the ring terminal of the jumper wire assembly to the *QuickScan80* ground terminal (identified as CP2 – GND). Attach the mini-clip end of the jumper wire assembly to resistor R42 at the position shown in Figure 2. Note difference in R42 location between early and later versions of the Gottlieb MPU.

Warning – Incorrect installation of the jumper wire assembly can result in damage to the MPU assembly and/or the QuickScan80. Only install or remove jumper wire only when power has been turned off.

The jumper wire assembly is not required if both U2 and U3 ROMs have been removed.

For System 80B machines:

The use of this jumper wire will not work on System 80B machines. For System 80B machines, either the 2764 EPROM must be removed from the daughter board or the entire daughter board must be removed. Also, PROM1 and/or PROM2 EPROM's must be removed (if present).

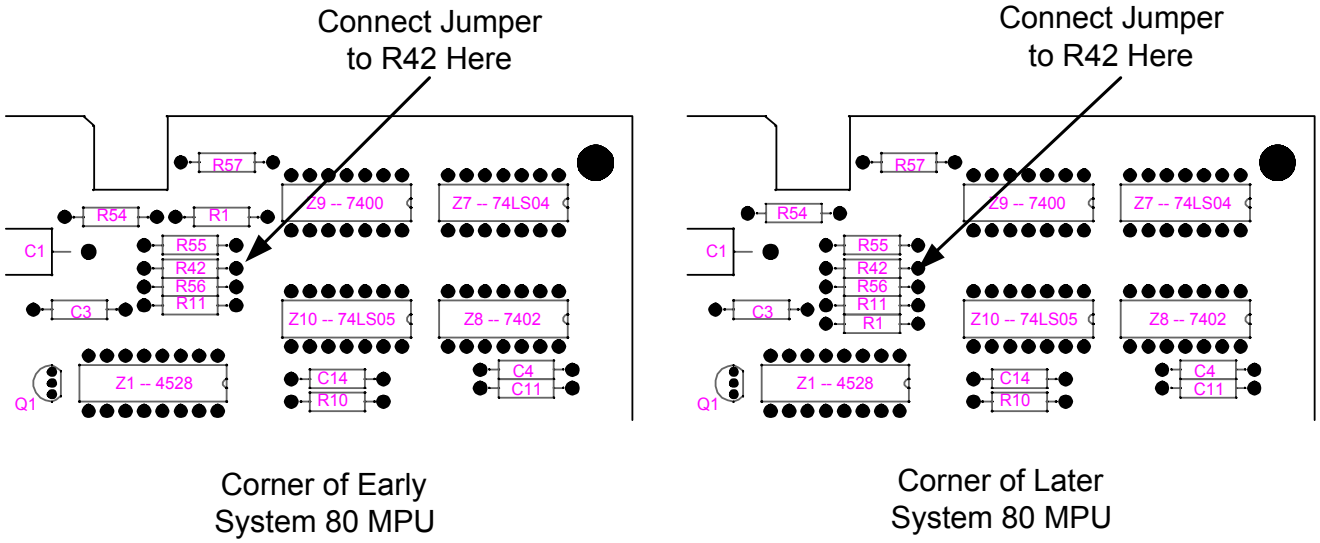


Figure 2 – Installation of Jumper assembly onto MPU R42.

Diagnostic Testing (Self-test) with the *QuickScan80*

Before testing can be performed, the *QuickScan80* must have proper Reset and Clock signals. Proper operation of these two signals can be quickly identified as a lit green Light Emitting Diode (LED) at both the CLOCK and RESET lamp positions. If either of these two LED's are red – the *QuickScan80* will be unable to operate and the offending signal will need to be repaired before testing can commence. The Interrupt Request (IRQ) LED's are provided for reference purposes. A red IRQ LED indicates a lack of Interrupt activity. A green IRQ indicates a presence of Interrupt activity. A lack of IRQ activity can indicate that either an IRQ is bad or can simply be that the software hasn't started the interrupt circuitry yet. During testing of the 5101, all interrupts are turned off.

Self-Test Sequence

Upon power up, the *QuickScan80* immediately enters the self-test mode. Self-test performs a number of different tests to verify the following devices and functions:

Self Test	7-Segment LED Display	Test Description
1	4	U4 – Quick test. Quick test to make sure U4 is alive and responsive.
2	5	U5 – Quick test. Quick test to make sure U5 is alive and responsive.
3	6	U6 – Quick test. Quick test to make sure U6 is alive and responsive.
4	1	Z5 – Quick test. Quick test to make sure Z5 is alive and responsive.
5	0	Interrupt test – Disable all RIOT interrupts and turn on CPU interrupt enable. If the QuickScan80 fails on this test then it has found an IRQ error but is unable to determine the source of this error.
6	4	U4 – Hex 55 Memory test. Writes and verifies a binary 01010101 pattern to all locations within RIOT memory.
7	4	U4 – Hex AA Memory test. Writes and verifies a binary 10101010 pattern to all locations within RIOT memory.
8	4	U4 – Random Memory test. Writes and verifies random data to all locations within RIOT memory.
9	4	U4 – Port B I/O test. Writes and verifies data at RIOT Port B. Port A is an input port only and cannot be tested.
10	4	U4 – Timer and IRQ test. Commands RIOT to perform multiple interrupts using RIOT timer and IRQ.
11	5	U5 – Hex 55 Memory test. Writes and verifies a binary 01010101 pattern to all locations within RIOT memory.
12	5	U5 – Hex AA Memory test. Writes and verifies a binary 10101010 pattern to all locations within RIOT memory.
13	5	U5 – Random Memory test. Writes and verifies random data to all locations within RIOT memory.
14	5	U5 – Port A I/O test. Writes and verifies data at RIOT Port A.
15	5	U5 – Port B I/O test. Writes and verifies data at RIOT Port B.
16	5	U5 – Timer and IRQ test. Commands RIOT to perform multiple interrupts using RIOT timer and IRQ.
17	6	U6 – Hex 55 Memory test. Writes and verifies a binary 01010101 pattern to all locations within RIOT memory.
18	6	U6 – Hex AA Memory test. Writes and verifies a binary 10101010 pattern to all locations within RIOT memory.
19	6	U6 – Random Memory test. Writes and verifies random data to all locations within RIOT memory.
20	6	U6 – Port A I/O test. Writes and verifies data at RIOT Port A.
21	6	U6 – Port B I/O test. Writes and verifies data at RIOT Port B.
22	6	U6 – Timer and IRQ test. Commands RIOT to perform multiple interrupts using RIOT timer and IRQ.
23	1	5101 – Hex 5 Memory test. Writes and verifies a binary 0101 pattern to all locations within 5101 memory.
24	1	5101 – Hex A Memory test. Writes and verifies a binary 1010 pattern to all locations within 5101 memory.
25	1	5101 – Random Memory test. Writes and verifies random data to all locations within 5101 memory.

After completion of testing, all data stored within the 5101 memory (Z5) is cleared. This means all high scores, credits, book keeping, and configuration data will be lost.

The 7-Segment display will show continuous status depending on which test is being performed. Tests 1 through 5 are normally performed quite rapidly and nothing will be seen on the display unless a test fails. A normally functioning board will display a sequence of "4…5…6…1… repeat". There is a short pause as each of the tests is performed. If a test fails, the ID of the device being tested begins slowly flashing with an alternating "F" to indicate the device is being continually retested.

Following testing of U6 – it is normal for the IRQ LED to show inactivity (red). Due to a circuitry time lag, this inactivity shows up during testing of Z5 ("1" on display) and overlaps testing of U4 ("4" on display).

After the final device (Z5, 5101) passes all tests, the *QuickScan80* examines the Start switch to determine if I/O testing is to be started (Start button pushed) or rerun self-test (Start button not pushed). Note – due to hardware and software requirements of the other test modes, all devices tested in self-test must completely pass testing before being allowed to enter I/O testing.

Input / Output (I/O) Testing with the *QuickScan80*

In addition to the Diagnostic self-testing, there are also five I/O tests for the *QuickScan80*. *QuickScan80* testing includes:

Test 2 – Lamp test – steps through all lamps turning them on then back off again.
Test 3 – Sound test – steps through sounds 1 through 16.
Test 4 – Solenoid test – steps through all solenoid drivers.
Test 5 – Switch test – scans through all possible switch positions.
Test 6 – Vacuum Fluorescent Display (VFD) test – sequentially displays test sequences thru VFD displays. This test is not performed when testing System 80B MPU's.

For System 80 and 80A machines, tests 2 through 6 will also display data on the game VFD displays. This functionality may be added for System 80B machines at a later date.
The speed of testing can be slowed down during tests 2 through 6 by using the game test button (just inside of coin door). Push and hold the test button until the test slows down. Repeat this to put the test back up to the full speed mode. If testing a System 80 or 80A game – a "1" or "2" will be shown in the lower ball count digit. A "1" signifies full speed and "2" signifies low speed.

Test 2 – Lamp Test

Upon entering Test 2, the *QuickScan80* sequentially displays "-2-" and then turns on and off each of the Lamp drivers. After the final lamp has been cycled, the *QuickScan80* examines the Start switch to determine if Test 3 should be started (Start pushed) or rerun Test 2 (Start not pushed).

System 80 and 80A machines will display the following on the game VFD displays:
Credit display = "2" signifying test number 2 – lamp test.
Status display (ball count) = test speed. 0 = Normal, 1 = Slow. Pushing and holding the machine's test button until the status display changes can change test speed.
Player 1 = Lamp Strobe value (DS1 – DS12)
Player 2 = Lamp Control value (LD1 – LD4)
Player 3 = Unused
Player 4 = Unused

MPU Circuitry tested specifically by Test 2:
Output port "B" of U6 -- 6532
Z32 – 7407 or 7417
Z33 – 74154, 74LS154 or 74HCT154
Z34 – 7404, 74LS04 or 74HCT04
Z35 – 7404, 74LS04 or 74HCT04

Note – Some sounds may be controlled by lamp control circuitry. This capability is game dependent.

Test 3 – Sound Test

Upon entering Test 3, the *QuickScan80* sequentially displays "-3-" and then steps though each of the primary 16 sound strobes. After completion of the primary 16 sounds, the *QuickScan80* toggles the Sound16 bit and tests the secondary 16 sounds. Due to an inconsistency with how the Sound16 and higher bits are allocated, the *QuickScan80* does not test higher than 16 sounds. After the final sound has been cycled, the *QuickScan80* examines the Start switch to determine if Test 4 should be started (Start pushed) or rerun Test 3 (Start not pushed).

System 80 and 80A machines will display the following on the game VFD displays:
Credit display = "3" signifying test number 3 – sound test.
Status display (ball count) = test speed. 0 = Normal, 1 = Slow. Pushing and holding the machine's test button until the status display changes can change test speed.
Player 1 = Sound value (0 thru 15)
Player 2 = Unused
Player 3 = Unused
Player 4 = Unused

MPU Circuitry tested specifically by Test 3:
Output port "A" of U6 -- 6532
Z27 – 7404, 74LS04 or 74HCT04
Z31 – 7408, 74LS08 or 74HCT08

Test 4 – Solenoid Test

Upon entering Test 4, the *QuickScan80* sequentially displays "-4-" and then turns on and off each of the nine dedicated solenoid drivers. After the final solenoid has been cycled, the *QuickScan80* examines the Start switch to determine if Test 5 should be started (Start pushed) or rerun Test 4 (Start not pushed).

System 80 and 80A machines will display the following on the game VFD displays:
Credit display = "4" signifying test number 4 – solenoid test.
Status display (ball count) = Unused.
Player 1 = Solenoid value (SOL1 – SOL9)
Player 2 = Unused
Player 3 = Unused
Player 4 = Unused

MPU Circuitry tested specifically by Test 4:
Output port "A" of U6 -- 6532
Z27 – 7404, 74LS04 or 74HCT04
Z28 – 74139, 74LS139 or 74HCT139
Z29 – 7406 or 7416
Z30 – 7406 or 7416

Test 5 – Switch Test

Upon entering Test 5, the *QuickScan80* sequentially displays "-5-" and then examines each of the possible 64 external switch locations. When a switch has been identified as closed, the *QuickScan80* displays "Cx-y" where x = column of switch closed and y = row of switch closed. For example, if the Start button is held, the displays will show "C4-7" for "Closed Column 4 Row 7". The column and row numbers can be easily translated into a switch identity through use of the specific game's manual. After the switch test has completely cycled through all 64 locations, the *QuickScan80* examines the Start switch to determine if Test 6 (Test 1 for System 80B testing) should be started (Start pushed) or rerun Test 5 (Start not pushed).

System 80 and 80A machines will display the following on the game VFD displays:
Credit display = "5" signifying test number 5 – switch test.
Status display (ball count) = Unused.
Player 1 = Column number of closed switch
Player 2 = Row number of closed switch
Player 3 = Value of slam switch. 0 = closed, 1 = open
Player 4 = Unused

MPU Circuitry tested specifically by Test 5:
Input port "A" and output port "B" of U4 – 6532
Output port "B" of U5 – 6532 (selects external switch matrix versus onboard DIP switches)
Output port "B" of U6 – 6532 (selects onboard DIP switch bank)
Z33 – 74154, 74LS154 or 74HCT154
Z11 – 7404, 74LS04 or 74HCT04
Z12 – 7404, 74LS04 or 74HCT04
Z13 – 7400, 74LS00 or 74HCT00
Z14 – 7400, 74LS00 or 74HCT00
Z15 – 7432, 74LS32 or 74HCT32
Also tested is Input port "A7" of U5 – Slam Switch
Z26, Section F – 7404, 74LS04 or 74HCT04 – Slam Switch

Test 6 – Game VFD Test

Upon entering Test 6, the *QuickScan80* immediately starts displaying a sequential count on the game's VFD displays. The 7-segment display on the *QuickScan80* will reflect what is being written to the VFD's. After the VFD test has cycled through numbers 0-9, the *QuickScan80* examines the Start switch to determine if self-test should be started (Start pushed) or rerun Test 6 (Start not pushed).

System 80 and 80A machines will display the following on the game VFD displays:
Credit display = numbers 0 through 9.
Status display (ball count) = numbers 0 through 9.
Player 1 = numbers 0 through 9
Player 2 = numbers 0 through 9
Player 3 = numbers 0 through 9
Player 4 = numbers 0 through 9

Note –Test 6 does not exist for System 80B games.

MPU Circuitry tested specifically by Test 6:
Output ports "A" and "B" of U5 -- 6532
Z16 – 7404, 74LS04 or 74HCT04
Z17 – 7404, 74LS04 or 74HCT04
Z18 – 74175, 74LS175 or 74HCT175
Z19 – 7448 or 74LS48
Z20 – 74175, 74LS175 or 74HCT175
Z21 – 7448 or 74LS48
Z22 – 74175, 74LS175 or 74HCT175
Z23 – 7448 or 74LS48
Z24 – 7404, 74LS04 or 74HCT04
Z25 – 74154, 74LS154 or 74HCT154
Z26 – 7404, 74LS04 or 74HCT04

ROM/PROM Emulation using the QuickScan80

In addition to being used as a test fixture, the *QuickScan80* can also be used as a ROM/EPROM emulator. This is useful if the System 80 or System 80A U2/U3 ROM's are missing or are of unknown working condition. To use the *QuickScan80* in a ROM emulation mode, install test fixture cables as described above. Next set the DIP switches to the following positions to use the game in ROM emulation mode. Note: In order for this function to operate, the user must program Gottlieb U2/U3 code into the *QuickScan80* EPROM (U1). This code is to be programmed into the EPROM at the following locations:

System 80 U2/U3 Code – 0x2000 through 0x3FFF
System 80A U2/U3 Code – 0x6000 through 0x7FFF

ROM Emulation DIP Switch settings:
Standard DIP Switch Settings for using QuickScan80 to emulate a system 80 ROM:

DIP Switch Position 1	ON (closed)
DIP Switch Position 2	ON (closed)
DIP Switch Position 3	OFF (open)
DIP Switch Position 4	ON (closed)

Standard DIP Switch Settings for using QuickScan80 to emulate a system 80A ROM:

DIP Switch Position 1	OFF (open)
DIP Switch Position 2	ON (closed)
DIP Switch Position 3	OFF (open)
DIP Switch Position 4	ON (closed)

Jumper setting:
For ROM emulation, the watchdog timer may be enabled if desired. Move Watchdog jumper to the *ON* position to enable the watchdog timer. Or leave the watchdog timer disabled with the jumper in the off position. The only time the watchdog timer is really needed is when a machine has problems with intermittent failures and is not being watched at all times. If the watchdog timer is disabled and the machine fails or "hangs", there is a risk that the machine could turn on a solenoid and leave it on – possibly resulting in a burnt solenoid and/or driver transistor.

Detailed Operation of the *QuickScan80*

The four-position DIP Switch on the *QuickScan80* is used to configure addressing modes of the test fixture as well as enabling/disabling the on board reset generator. DIP Switches 1 and 2 selects which set of *QuickScan80* code will be inserted into the upper address space of the MPU (0x2000 through 0x3FFF). This MPU address space is typically reserved for the Gottlieb U2 and U3 ROM's of the System 80 and 80A boards and the daughter board 2764 EPROM of the System 80B boards. These switches allow the user to select one of four pages of *QuickScan80* memory to appear within the System 80 MPU's upper address space:

Switch 1	Switch 2	Switch 3	Code executed by MPU:	*QuickScan80* EPROM Address Space
ON (closed)	ON (closed)	OFF (open)	U2 & U3 System 80 Code (User installed code)	0x2000 – 0x3FFF
OFF (open)	ON (closed)	OFF (open)	U2 & U3 System 80A Code (User installed code)	0x6000 – 0x7FFF
ON (closed)	OFF (open)	OFF (open)	System 80B Self Test Code	0xA000 – 0xBFFF
OFF (open)	*OFF (open)*	*OFF (open)*	System 80/80A Self Test Code	0xE000 – 0xFFFF

Notes:

- U2 & U3 code for System 80 and 80A machines are copyrighted by Gottlieb® and are not provided with this test fixture.
- Default values are shown in italics – three switches OFF or open.

DIP Switch 3 is used for selecting an extended addressing mode. When DIP Switch 3 is OFF or open, extended addressing mode is off (default position). Turning extended addressing mode on (Dip switch ON or closed) enables the test fixture to insert code whenever the CPU is accessing the game specific PROM locations – located within MPU address space 0x1000 through 0x17FF. This allows the user to program the test fixture to emulate the game specific PROM's. With the proper code programmed into the *QuickScan80* test fixture, a Gottlieb MPU can control a pinball machine without any original ROM's or PROM's located on the MPU. The extended addressing ranges within the QuickScan80 EPROM depend on the setting of Switches 1 and 2. Refer to the following table for extended address locations within the QuickScan80 EPROM Address space:

Switch 1	Switch 2	Switch 3	Game Code executed by MPU:	*QuickScan80* EPROM Address Space
ON (closed)	ON (closed)	ON (closed)	System 80 Game code (User Installed code)	0x1000 – 0x17FF
OFF (open)	ON (closed)	ON (closed)	System 80A Game Code (User Installed code)	0x5000 – 0x57FF
ON (closed)	OFF (open)	ON (closed)	Not Allowed	0x9000 – 0x97FF
OFF (open)	OFF (open)	ON (closed)	Not Allowed	0xD000 – 0xD7FF

Notes:

- Game code for System 80 and 80A machines are copyrighted by Gottlieb® and are not provided with this test fixture.
- Game Code must be programmed per specific game.

Important!

Extended addressing must never be turned ON (DIP Switch 3 closed) whenever an MPU game PROM (PROM1 or PROM2) is installed.

DIP Switch 4 is used for enabling or disabling the *QuickScan80* on board reset generator. Opening DIP Switch 4 disables the reset function, the watchdog timer and the on-board reset switch of the *QuickScan80* test fixture. Closing DIP Switch 4 enables the reset function, the watchdog timer and the on-board reset switch. The default position for this switch is ***ON*** or closed. A remote reset button is provided on the QuickScan80 to allow the user to reset the MPU without toggling the main power switch on the pinball machine. The watchdog timer can be turned off separately through the use of the watchdog jumper.

Starting with the later of the System 80A machines and continuing through the System 80B machines - Gottlieb® installed a remote reset board which monitored activity on the CPU board and issued a reset whenever the CPU was believed to be locked up. This function is commonly referred to as a watchdog timer. The *QuickScan80* test fixture has the capability to perform a similar function through the use of its own watchdog timer. This watchdog timer monitors the IRQ activity from the RIOT's and issues a reset to the MPU board if the activity stops for an extended period of time. A two-position jumper is used on the *QuickScan80* to enable/disable the watchdog timer function without affecting the operation of the Reset Switch. ***Whenever the QuickScan80 is used for testing purposes – the watchdog timer function must be disabled (turned off).*** Whenever the QuickScan80 is used for ROM / PROM emulation, the watchdog timer function should be enabled but doesn't need to be. Control of the watchdog timer function is performed by locating the jumper on either the ON position (enabled) or the OFF position (disabled).

Existing Reset Board

As stated before, Gottlieb® installed a remote reset board on its later series of System 80 pinball machines. This reset board must be removed prior to the original Gottlieb® remote reset board.

Connecting Auxiliary Power installation of the QuickScan80.

The *QuickScan80* obtains its operating power through the ribbon cable assembly. As an option, power can also be provided to the *QuickScan80* through the use of the two power terminals – CP1 and CP2. Connect the VCC terminal (CP1) to an appropriate +5Volt connection point on the MPU or Voltage Regulator assembly. Connect the GND terminal (CP2) to an appropriate ground connection point on the MPU or Voltage Regulator assembly. This is the recommended method of providing power to the *QuickScan80* if it is to be left in a machine for an extended period of time.

Test Conditions and Trouble Shooting Using the *QuickScan80*

Although the *QuickScan80* has been created to be as thorough as possible in it's testing, there are conditions where the *QuickScan80* cannot identify the problem or may even misidentify the problem. There are also several conditions that must be satisfied before the *QuickScan80* can even begin to start testing of the MPU assembly.

Startup Conditions

There are a number of start up conditions that must be satisfied before testing can begin, these conditions include:

1 +5volt Power must be within **5%**.
2 The MPU clock must be running properly (as indicated by CLOCK LED's).
3 The MPU reset must be operating properly (as indicated by RESET LED's).
4 The MPU address and data lines must be operating properly.
5 The MPU decode logic must be operating properly.
6 The 6502 CPU itself must be operating properly

Most of the electronic devices on the MPU expect the power to be +5 Volts +/-5%. If the voltage is too low, the MPU cannot possibly function properly. If the voltage is too high, damage to MPU components and/or the *QuickScan80* can occur. Also, verify proper operation of the power supply main filter capacitor. If this capacitor is 10 or more years old or is passing too much AC ripple voltage then it must be replaced.

The MPU clock must be running at its nominal speed of 895KHz. Check CPU pin 37 for presence of the clock (as indicated by CLOCK LED). When an MPU clock is not working properly, it is usually due to battery corrosion problems within the clock circuitry.

The MPU clock circuitry includes:

Y1 – Crystal, 3.579545MHz, parallel resonance
Z2 – Integrated Circuit, Dual D-Type Flip-Flop – Part type 7474, 74LS74, or 74HCT74
Z3 – Integrated Circuit, Hex Inverter – Part type 7404
R3 – Resistor, 5.6K ohm, ¼ Watt
R4 – Resistor, 2K ohm, ¼ Watt
R5 – Resistor, 2K ohm, ¼ Watt

The MPU reset must pulse low at power up and must rise and stay high after approximately 100mS following power up. If the MPU reset is not working properly, it could be due to battery corrosion problems within areas of the MPU reset circuitry.

The MPU reset circuitry includes:

- C3 – Capacitor, Ceramic, 0.1uF
- C14 – Capacitor, Ceramic, 0.1uF
- C25 – Capacitor, Ceramic, 0.1uF
- C36 – Capacitor, Tantalum, 10uF, 10 Volt (typical)
- Z1 – Integrated Circuit, Dual Monostable Multivibrator – Part type 4528
- Z4 – Integrated Circuit, Quad 2-Input AND Gate – Part type 4081
- R7 – Resistor, 62 ohm, ¼ Watt
- R8 – Resistor, 180 ohm, ¼ Watt
- R9 – Resistor, 1K ohm, ¼ Watt
- R10 – Resistor, 2.7M ohm, ¼ Watt
- R43 – Resistor, 5.6K ohm, ¼ Watt
- R44 – Resistor, 2K ohm, ¼ Watt
- R45 – Resistor, 3K ohm, ¼ Watt
- R46 – Resistor, 3K ohm, ¼ Watt
- R47 – Resistor, 24K ohm, ¼ Watt
- R48 – Resistor, 3K ohm, ¼ Watt
- R49 – Resistor, 5.6K ohm, ¼ Watt
- R50 – Resistor, 180 ohm, ¼ Watt
- Q1 – Transistor, PNP – Part type MPS-A70 (Alternate 2N4403)
- Q2 – Transistor, NPN – Part type 2N4400 (Alternate 2N4401)
- Q3 – Transistor, NPN – Part type 2N4400 (Alternate 2N4401)
- Q4 – Transistor, PNP – Part type MPS-A70 (Alternate 2N4403)
- VR1 – Diode, Zener, 3 Volt – Part type 1N5225B
- CR33 – Diode, Switching – Part type 1N4148
- CR34 – Diode, Switching – Part type 1N4148
- CR35 – Diode, Switching – Part type 1N4148

The MPU address and data lines must be functioning properly. Verify that none are open or shorted to each other or other signals. Opens are usually due to scratches to the PC board, cracked solder joints, poor IC socket condition or battery corrosion damage. Shorts are usually due to bad solder joints, solder splashes, or stray pieces of wire present on the PC board.

The MPU decode logic must also be functioning properly. This is impossible to visually examine as this normally happens as a result of a defective address decoder component. Due to the fact that CMOS circuitry (4000 series part numbers) is used in the decode logic, this circuitry is easily damaged by the slightest static electricity shock. Also, some of the MPU decode logic lies within the dreaded ‘battery corrosion zone’. Defective decode logic can frequently turn on more than one device at a time and can sometimes be identified as erratic operation of the MPU or a dead MPU.

The MPU decode logic includes:

- Z4 – Integrated Circuit, Quad 2-Input AND Gate – Part type 4081
- Z7 – Integrated Circuit, Hex Inverter – Part type 74LS04
- Z8 – Integrated Circuit, Quad 2-Input NOR Gate – Part type 7402
- Z9 – Integrated Circuit, Quad 2-Input NAND Gate – Part type 7400
- Z10 – Integrated Circuit, Hex Inverter – Part type 74LS05
- Z12 – Integrated Circuit, Hex Inverter – Part type 7404
- Z36 – Integrated Circuit, Hex Inverter – Part type 4069
- R11 – Resistor, 3K ohm, ¼ Watt
- R42 – Resistor, 3K ohm, ¼ Watt
- R54 – Resistor, 3K ohm, ¼ Watt
- R55 – Resistor, 3K ohm, ¼ Watt
- R56 – Resistor, 3K ohm, ¼ Watt
- R57 – Resistor, 3K ohm, ¼ Watt

And lastly, the 6502 processor itself (U1) must be functioning properly. This is also impossible to visually examine. It can also be identified as erratic operation of the MPU or a dead MPU. If this behavior is noted – first examine solder joints to all decode logic and the CPU. If none is found, then the either the CPU or devices in one of the above areas of logic are suspect.

Erroneous Status Conditions

There are a few conditions that exist that can allow the *QuickScan80* to provide erroneous failure notifications.

Known conditions include:

1 If a RIOT or memory (5101 or PROM) has defective decode or enable logic, the first RIOT tested (U4) will usually (but not always) be flagged as a failed RIOT. This will be apparent when the problem persists after U4 has been replaced with a known good device.

Handling and storage of the QuickScan80

Like most electronic assemblies, the *QuickScan80* is comprised of static sensitive components. Proper handling precautions must be used to avoid damaging the MPU and/or the *QuickScan80.* Always use a grounded static strap when working with static sensitive assemblies and always store the assemblies in static shielding bags when not in use.

Disclaimers

Due to the harsh nature of the equipment being tested by the *QuickScan80,* the wide range of failed components being tested and the wide range of user technical capabilities – Great Plains Electronics can not be held responsible for any damage caused to the *QuickScan80* or caused by the use of the *QuickScan80*.

The *QuickScan80* has been created to assist in the repair of electronic pinball machines. Great Plains Electronics shall assume no liability for any application of the QuickScan80 when used beyond its intended purpose.

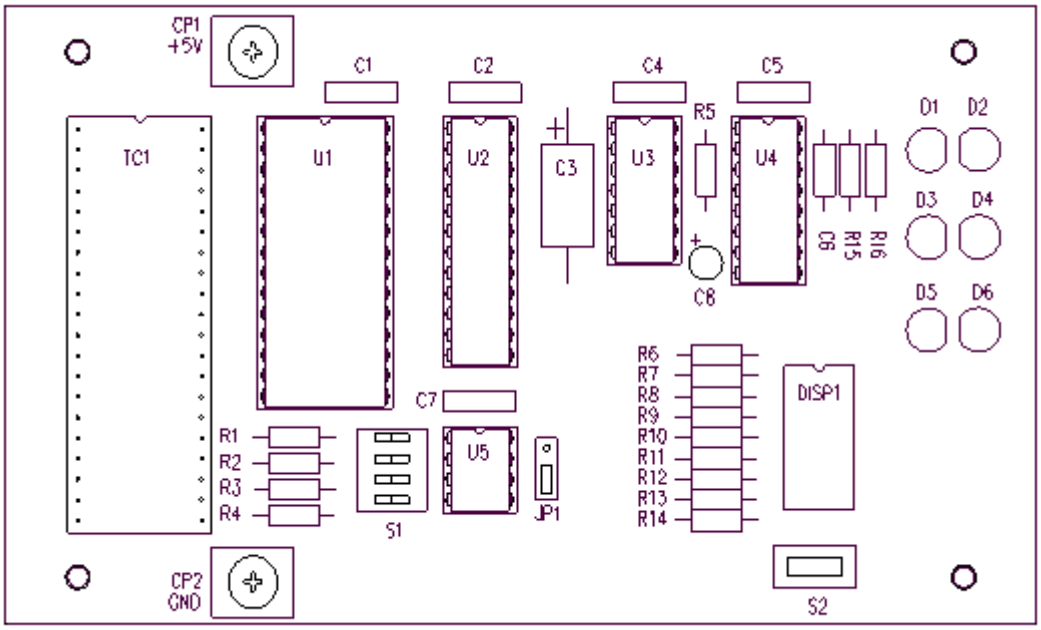
We reserve the right to make product upgrades, changes, and improvements to our products at any time without any requirement to provide these same upgrades, changes, or improvements to previously manufactured and/or delivered products.

Warranty

The *QuickScan80* is guaranteed to be free of manufacturer defects for a period of 1 year from date of purchase. This warranty applies to the original purchaser only and is not transferable. Warranty is void if someone other than Great Plains Electronics attempts repairs or modifications to this test fixture. Repairs performed under warranty do not extend the original 1-year warranty period. Great Plains Electronics reserves the exclusive rights to determine cause of failures and if the failure is covered by our warranty.

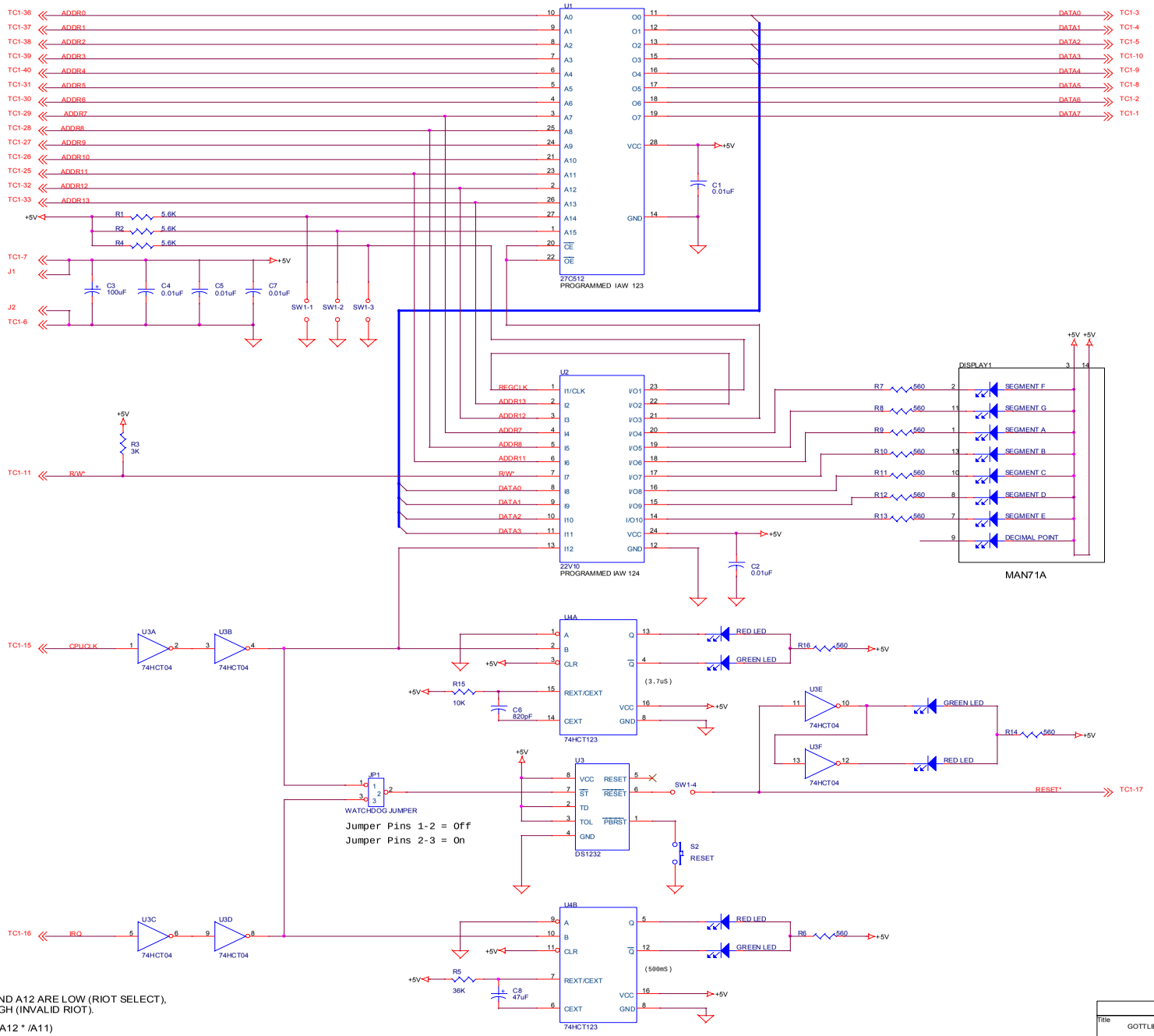
Due to the limited life span of ribbon type cable assemblies – the ribbon cable assembly provided with the *QuickScan80* is NOT covered by any type of warranty.

Appendix A – Assembly Drawing and Parts List



Item	Quantity	Part Number	Description	Reference
1	1	121-003	Printed Circuit Board, System 80 Text Fixture	
2	1	27C512	Integrated Circuit, Memory, EPROM, 64K x 8	U1
3	1	GAL6001B-30LP	Integrated Circuit, Generic Array Logic	U2
4	1	74HCT04	Integrated Circuit, Hex Inverter	U3
5	1	74HCT123	Integrated Circuit, Dual Retriggerable One-Shot	U4
6	1	DS1232-LP	Integrated Circuit, Reset Generator	U5
7	1	MAN71A	LED Display, 7-Segment, Common Anode	DISP1
8	3	LED-GRN	LED, Green, Diffused, Size T1-3/4	D2, 4, 6
9	3	LED-RED	LED, Red, Diffused, Size T1-3/4	D1, 3, 5
10	1	206-4	DIP Switch, 4 Position	S1
11	1	TL1107	Push Button Switch, Momentary	S2
12	3	RCF1/4-5.6K	Resistor, 5.6K ohm, ¼ Watt	R1, 2, 4
13	1	RCF1/4-3.0K	Resistor, 3.0K ohm, ¼ Watt	R3
14	1	RCF1/4-36K	Resistor, 36K ohm, ¼ Watt	R5
15	10	RCF1/4-560	Resistor, 560 ohm, ¼ Watt	R6-14, 16
16	1	RCF1/4-10K	Resistor, 10K ohm, ¼ Watt	R15
17	5	CCD-0.01uF-50v	Capacitor, Ceramic, 0.01uF	C1, 2, 4, 5, 7
18	1	CEA-100uF-10v	Capacitor, Electrolytic, 100uF	C3
19	1	CCA-820pF-50v	Capacitor, Ceramic, 820pF	C6
20	1	CER-47uF-25v	Capacitor, Electrolytic, 47uF	C8
21	2	8191	Screw Terminal, PCB Mount	CP1, 2
22	4	SRS6-8-01	PCB Standoff, Nylon, #4 x ½ Inch	
23	1	IS-640-MP	IC Socket, 40 Pin, 0.6 Inch	TC1
24	1	IS-628-MP	IC Socket, 28 Pin, 0.6 Inch	XU1
25	1	IS-324-MP	IC Socket, 24 Pin, 0.3 Inch	XU2
26	1	IS-314-MP	IC Socket, 14 Pin, 0.3 Inch	XU3
27	1	IS-316-MP	IC Socket, 16 Pin, 0.3 Inch	XU4
28	1	IS-308-MP	IC Socket, 8 Pin, 0.3 Inch	XU5
29	1	PH1-103S-G	Header, 1 x 3	JP1
30	1	MJ6.47C-G	Jumper, 0.1 Inch	JP1

Appendix B – Schematic Diagram



WRITE TO 7-SEG WHEN A13 AND A12 ARE LOW (RIOT SELECT),
AND WHEN A8 AND A7 ARE HIGH (INVALID RIOT).

SELECT ROM @ A13 or (/A13 * A12 * /A11)

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